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IBM Builds Super-Dense 5-Nanometer Chip

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Two years after IBM created the first 7-nanometer chip, it has announced a new breakthrough process to build an even more densely-packed chip, one measuring only 5 nm.

How Big Is A 5 Nanometer Chip?

A human hair is about 100,000 nanometers thick. A strand of DNA is about 2.5 nanometers in diameter. The new IBM 5 nm chip is therefore about as wide as two strands of DNA. About 30 billion 5 nm switches can be packaged onto a chip the size of a fingernail.

The smallest and most advanced chips commercially available today are about 10 nm. The recently announced 5 nm chip is the smallest silicon processor ever produced.

What Are The Advantages of Such a Small Chip?

The more densely transistors are packed onto a chip, the closer together they are. Therefore, signals can pass between the transistors more rapidly. A 5 nm chip achieves a 40% boost in performance as compared to a 7 nm chip. Alternatively, the 5 nm chip can provide the same performance while using 75% less power.

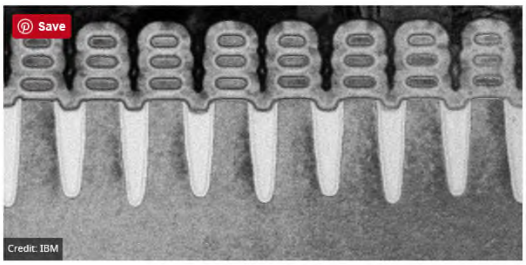
Such a power savings means that batteries in smartphones and other mobile products could last two to three times longer on a charge, a real boon to mobile users (which most of us now are).

How Did IBM Achieve Such a Small Chip Size?

IBM said three years ago that it would invest $3 billion over five years in chip research and development. IBM Research has more than 3,000 researchers in 12 labs. The 5 nm transistor is a product of this research effort.

Current transistors are made with what is known as the FinFet architecture. This model is named for the fin-like ridges of silicon that project from the chip's surface. Transistors are fin-shaped with three current-carrying channels surrounded by an insulating layer. The fins are surrounded on their three exposed sides by a structure called a 'gate.' The gate switches the flow of current on and prevents electrons from leaking out when the transistor is off.

The FinFet architecture is used in 10 nm and 7 nm transistors. However, these transistors are bumping up against limits as to how far down they can be scaled. At 5nm, the gates are not totally effective; and electrons leak out.



FinFet Transistors (Forbes)

IBM has been researching a new technology for making smaller transistors for over a decade. This new technique uses stacked silicon nanosheets to pack transistors more closely. By stacking the nanosheets on top of each other, massive numbers of transistors are positioned closely to each other.

In IBM's new design, each transistor is made up of four stacked horizontal sheets of silicon, each only a new nanometers thick. Each transistor is completely surrounded by gates to control current flow. The nanosheets range from 8 to 50 nm wide. The wider the sheet, the better the performance; but power requirements increase.

The new process is called 'gate-all-around' (GAA) transistors. The horizontal layers of stacked silicon enable a fourth gate for the transistors on the chip. Signals can be sent through all four gates at once.

To create the transistors on a silicon sheet, IBM uses Extreme Ultraviolet (EUV) lithography to write patterns on a silicon wafer using a much higher wavelength of light. Using this technique, finer details can be created on a chip.

When Will the 5 nm Chips Be Available?

The 5 nm chip is coming out of IBM's Research Alliance with chip foundry partners GlobalFoundaries and Samsung. IBM does not manufacture chips anymore, but the others in its alliance do.

It will still be a while before 5 nm chips becomes commercially available. 10 nm chips are now just reaching the marketplace. 7 nm chips are due for commercial release in 2019. 5 nm chips are still about four years away.

Moore's Law

This kind of achievement should enable the $330 billion chip industry to stay on the path of Moore's law. In 1965, Gordon Moore, a co-founder of Intel, predicted that the number of transistors per square inch would double about every two years.

After more than five decades, we are still on the track predicted by Moore.

Summary

Smaller and smaller chips are arriving with some regularity. 10 nm transistors have been around for some time. 7 nm transistors are expected to be commercially available in 2019. They can cram 20 billion transistors onto a chip the size of a fingernail, Now 5 nm transistors are expected in the early 2020s.

Will this trend continue? We'll have to wait and see, but based on the never-ending forward march of technology, we are likely to see even smaller transistors in the not-to-distant future.

Acknowledgements

Information for this article was taken from the following sources:

IBM's new 5nm architecture crams 30 billion transistors onto fingernail-sized chip, *NewAtlas*; June 4, 2017.
Research creates a groundbreaking 5-nanometer chip, *VentureBeat*; June 4, 2017.
IBM Shows The World How To Build A Super Dense 5-Nanometer Chip, *Forbes*; June 5, 2017.
IBM creates a new transistor type for 5nm silicon chips, *TechCrunch*; June 5, 2017.
Nanosheets: IBM's Path to 5-Nanometer Transistors, *Spectrum*; June 5, 2017.